CLAIMS

1. A n-type group III nitride semiconductor layered structure comprising a substrate and, stacked on the substrate, an n-type impurity concentration periodic variation layer comprising an n-type impurity atom higher concentration layer and an n-type impurity atom lower concentration layer, said lower concentration layer being stacked on said higher concentration layer.

2. The n-type group III nitride semiconductor layered structure according to claim 1, wherein said n-type impurity atom is one element or a combination of at least two elements selected from the group consisting of silicon (Si), germanium (Ge), sulfur (S), selenium (Se), tin (Sn), and tellurium (Te).

3. The n-type group III nitride semiconductor layered structure according to claim 2, wherein said n-type impurity atom is Ge.

4. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 3, wherein pits are provided on a surface of the higher concentration layer (a surface remote from the substrate).

5. The n-type group III nitride semiconductor layered structure according to claim 4, wherein the number of pits formed is in the range of $1 \times 10^5/cm^2$ to $1 \times 10^{10}/cm^2$.

6. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 5, wherein the flatness (Ra) of the surface of the lower concentration layer (a surface remote from the substrate) is not more than 10 angstroms.

7. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 6, wherein the higher concentration layer and the lower concentration layer are provided in an alternate and periodic manner.

8. The n-type group III nitride semiconductor

layered structure according to any one of claims 1 to 7, wherein the thickness of the higher concentration layer and the thickness of the lower concentration layer each are 0.5 to 500 nm.

9. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 8, wherein the thickness of the lower concentration layer is equal to or larger than the thickness of the higher concentration layer.

10. The n-type group III nitride semiconductor layered structure according to any one of claims 7 to 9, wherein the repetition number of said higher concentration layer and said lower concentration layer is 10 to 1000.

11. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 10, wherein the thickness of the n-type impurity concentration periodic variation layer is 0.1 to 10 μm.

12. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 11, wherein the concentration of the n-type impurity in the higher concentration layer is $5 \times 10^{17}$ to $5 \times 10^{19}$ $cm^{-3}$.

13. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 12, wherein the concentration of the n-type impurity in the lower concentration layer is lower than the concentration of the n-type impurity in the higher concentration layer and is not more than $2 \times 10^{19}$ $cm^{-3}$.

14. The n-type group III nitride semiconductor layered structure according to claim 13, wherein the n-type impurity is not intentionally doped into the lower concentration layer.

15. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 14, which comprises a base layer, having a lower carrier concentration than the n-type impurity concentration

periodic variation layer, between said substrate and said n-type impurity concentration periodic variation layer.

16. The n-type group III nitride semiconductor layered structure according to claim 15, wherein said base layer contains an n-type impurity as a dopant and the concentration of the n-type impurity is not more than $5 \times 10^{18}$ $cm^{-3}$.

17. The n-type group III nitride semiconductor layered structure according to claim 15, wherein said base layer is undoped.

18. The n-type group III nitride semiconductor layered structure according to any one of claims 15 to 17, wherein the thickness of the base layer is not less than 1 μm and not more than 20 μm.

19. The n-type group III nitride semiconductor layered structure according to claim 18, wherein the thickness of the base layer is not less than 5 μm and not more than 15 μm.

20. The n-type group III nitride semiconductor layered structure according to any one of claims 15 to 19, wherein the carrier concentration of the base layer is not more than $5 \times 10^{17}$ $cm^{-3}$.

21. The n-type group III nitride semiconductor layered structure according to any one of claims 1 to 20, wherein the plane direction of the surface of the substrate is slightly inclined with respect to the just direction.

22. The n-type group III nitride semiconductor layered structure according to claim 21, wherein the plane direction of the surface of the substrate is inclined by 0.05 to 0.6 degree with respect to the just direction.

23. The n-type group III nitride semiconductor layered structure according to claim 21 or 22, wherein said substrate is selected from the group consisting of oxide single crystal materials such as sapphire ($\alpha$-$Al_2O_3$

single crystal), zinc oxide (ZnO), and gallium lithium oxide ($LiGaO_2$), group IV semiconductor single crystals including silicon (Si) single crystals (silicon) and cubic or hexagonal silicon carbide (SiC), and group III-V compound semiconductor single crystals including gallium phosphide (GaP), gallium arsenide (GaAs), and gallium nitride (GaN).

24. A process for producing a n-type group III nitride semiconductor layered structure according to any one of claims 1 to 23, wherein each of said n-type impurity atom higher concentration layer and said n-type impurity atom lower concentration layer is stacked so that, in addition to the concentration of the n-type impurity to be doped, conditions for growth within a reactor are also differentiated.

25. The process according to claim 24, wherein conditions for growth of the lower concentration layer are differentiated from conditions for growth of the higher concentration layer so that two-dimensional growth of the layer is accelerated during the growth of the lower concentration layer.

26. The process according to claim 24 or 25, wherein the lower concentration layer is grown at a temperature different from the temperature at which the higher concentration layer is grown.

27. The process according to claim 26, wherein the lower concentration layer is grown at a temperature above the temperature at which the higher concentration layer is grown.

28. The process according to any one of claims 24 to 27, wherein the lower concentration layer is grown at a pressure different from the pressure at which the higher concentration layer is grown.

29. The process according to claim 28, wherein the lower concentration layer is grown at a pressure lower than the pressure at which the higher concentration layer is grown.

30. The process according to any one of claims 24 to 29, wherein the carrier gas flow rate in the growth of the lower concentration layer is different from the carrier gas flow rate in the growth of the higher concentration layer.

31. The process according to claim 30, wherein the carrier gas flow rate in the growth of the lower concentration layer is higher than the carrier gas flow rate in the growth of the higher concentration layer.

32. The process according to any one of claims 24 to 31, wherein the growth speed of the lower concentration layer is different from the growth speed of the higher concentration layer.

33. The process according to claim 32, wherein the growth speed of the lower concentration layer is lower than the growth speed of the higher concentration layer.

34. The process according to any one of claims 24 to 33, wherein the nitrogen/III ratio in the growth of the lower concentration layer is different from the nitrogen/III ratio in the growth of the higher concentration layer.

35. The process according to claim 34, wherein the nitrogen/III ratio in the growth of the lower concentration layer is lower than the nitrogen/III ratio in the growth of the n-type impurity atom higher concentration layer.

36. A group III nitride semiconductor light-emitting device comprising a light-emitting layer composed of a group III nitride semiconductor provided on the substrate, wherein the n-type group III nitride semiconductor layered structure according to any one of claims 1 to 23 is provided between the substrate and the light-emitting layer.